IN THE CLAIMS:

Please amend claims 12, 25, and 26 as indicated in the following.

Please add new claims 36-65 as indicated in the following.

Claims Listing:

1. – 11. (Canceled)

12. (Currently Amended) A system comprising:

a data processor ~~having a first I/O buffer~~;

a memory ~~having a second I/O buffer~~ coupled to ~~the first I/O buffer of~~ the data processor,

the memory ~~capable of~~ for storing code for:

establishing a set of encrypted links between a peripheral device and a software component, wherein establishing a first encrypted link of the set of encrypted links includes generating a first encryption key associated with a first port of encrypted data and establishing a second encrypted link of the set of encrypted links includes generating a second encryption key associated with a second port of encrypted data;

a hardware controller ~~capable of~~for outputting the first and the second encrypted links,

wherein the hardware controller includes:

a first register ~~capable of~~ for storing information associated with the first encryption key;

a second register ~~capable of~~for storing information associated with the second encryption key;

a cipher component ~~capable of~~ for:

receiving a single digital data stream;

applying the first encryption key to a first portion of the data stream; and

applying the second encryption key to a second portion of the data stream; and

a de-multiplexing component ~~capable of~~for splitting the single data stream into multiple data streams.

13. – 24. (Canceled)

25. (Currently Amended) A system comprising:

an interface ~~capable of~~ for receiving a first link of encrypted data and a second link of encrypted data from a hardware controller;

a first decryption component ~~capable of~~for decrypting the first link of encrypted data[[,]] using a first encryption key[[,]] to generate a first portion of a single received digital data stream;

a second decryption component ~~capable of~~ for decrypting the second link of encrypted data using a second encryption key to generate a second portion of the received digital data stream; and

a multiplexing component ~~capable of~~for combining the first and the second portions of the received data streams to form a single received digital data stream.

26. (Currently Amended) The system as in Claim 25, further including:

a clock ~~capable of~~for clocking the single received data stream at twice the speed of the first and second links of encrypted data; and

a single processing component ~~capable of~~ for processing the data associated with the first and the second links of encrypted data.

27. – 35. (Canceled)

36. (New) The system as in Claim 25, wherein the interface is further for receiving a horizontal sync signal.

37. (New) The system as in Claim 36, wherein the first and the second encryption keys are regenerated according to the horizontal sync signal.

38. (New) The system as in Claim 25, wherein the multiplexing component assigns bits of data in the first portion of the received data stream to even pixels in the received data stream and assigns bits of data in the second portion of the received data stream to odd pixels in the received data stream.

39. (New) The system as in Claim 25, wherein the hardware controller is a video controller.

40. (New) The system as in Claim 39, wherein the first and the second link of encrypted data are transmitted from a dual link digital video output (DVO) port on the video controller that is capable of outputting two links of data related to video.

41. (New) The system as in Claim 25, wherein the first portion of the received digital data stream is associated with even pixels and the second portion of the received digital data stream is associated with odd pixels.

42. (New) The system as in Claim 12, further comprising:

a multiplexing component capable of:

combining the information stored in the first register with the information stored in the second register; and

providing the combined information to the cipher component;

a clock capable of clocking data bits from the single data stream; and

a half speed clock capable of clocking data in the multiple data streams.

43. (New) The system as in Claim 12, wherein the cipher component applies the first encryption key to even bits in the single data stream and applies the second encryption key to odd bits in the single data stream.

44. (New) The system as in Claim 12, further comprising a peripheral device comprising:

an interface for receiving the multiple data streams;

a first decryption component for decrypting a first data stream of the multiple data streams to generate a first decrypted data stream;

a second decryption component for decrypting a second data stream of the multiple data streams to generate a second decrypted data stream; and

a multiplexing component for combining the first and the second decrypted data streams to generate a single decrypted data stream.

45. (New) The system as in Claim 44, wherein the interface is further for receiving a horizontal sync signal.

46. (New) The system as in Claim 45, wherein the first and second encryption keys are regenerated according to the horizontal sync signal.

47. (New) The system as in Claim 12, wherein the hardware controller is a video controller.

48. (New) The system as in Claim 47, wherein the multiple data streams are received from a dual link digital video output (DVO) port on the video controller that is capable of outputting two channels of data related to video.

49. (New) The system as in Claim 48, wherein the multiple data streams are transmitted using a transmission-minimized differential signaling (TMDS) transmitter.

50. (New) The system as in Claim 49, further including a TMDS receiver capable of receiving the transmitted data associated with the multiple data streams and outputting the multiple data streams.

51. (New) The system as in Claim 12, wherein the multiple data streams are received from a dual link internal TMDS transmitter and transmitted using a video interface capable of outputting two channels of pixel data related to video.

52. (New) The system as in Claim 12, wherein the first portion of the digital data stream is associated with even pixels and the second portion of the data stream is associated with odd pixels.

53. (New) A method comprising:

receiving a data stream comprising display data representative of video to be displayed;

encrypting a first portion of the display data using a first encryption key to generate a first encrypted stream;

encrypting a second portion of the display data using a second encryption key to generate a second encrypted stream;

transmitting the first encrypted stream for reception by a peripheral device via a first link of a video output port; and

transmitting the second encrypted stream for reception by the peripheral device via a second link of the video output port that is separate from the first link of the video output port.

54. (New) The method as in Claim 53, wherein encrypting the first portion of the display data and encrypting the second portion of the display data is performed by the same encryption component.

55. (New) The method as in Claim 53, further comprising:

generating the first encryption key using a public encryption key associated with the peripheral device, a private key associated with the peripheral device, and a first pseudo random number; and

generating the second encryption key using the public encryption key associated with the peripheral device, the private key associated with the peripheral device, and a second pseudo random number.

56. (New) The method as in Claim 53, further comprising:

receiving the first encrypted stream and the second encrypted streams at the peripheral device;

decrypting the first encrypted stream to generate a first portion of a received display data;

decrypting the second encrypted stream to generate a second portion of the received display data; and

combining the first portion of the received data stream with the second portion of the received display data to generate a received video stream.

57. (New) The method as in Claim 56, further comprising:
storing the received video stream at the peripheral device.

58. (New) The method as in Claim 56, further comprising:
displaying video represented by the received video stream at the peripheral device.

59. (New) The method as in Claim 53, further comprising:
receiving a horizontal sync signal at the peripheral device via the video output port; and
regenerating at least one of the first encryption key and the second encryption key at the peripheral device in response to the horizontal sync signal.

60. (New) The method as in Claim 53, wherein the first portion of the display data comprises data representative of even pixels of the display data and the second portion of the display data comprises data representative of odd pixels of the display data.

62. (New) The method as in Claim 53, wherein:
encrypting the first portion of the display data comprises encrypting even bits of the display data with the first encryption key; and
encrypting the second portion of the display data comprises encrypting odd bits of the display data with the second encryption key.

63. (New) The method as in Claim 53, wherein the peripheral device comprises a display device.

64. (New) The method as in Claim 53, wherein the video output port comprises a DVI-compatible video output port.

65. (New) The method as in Claim 53, wherein the first link comprises a first video data link of the DVI-compatible video output port and the second link comprises a second video data link of the DVI-compatible video output port.